In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 8, line 26 to page 9, line 9 as follows:

-- The DMA controllers 18, 28 preferably assert request (REQ) signals to the arbiter 136 when they desire access to the XPORT. The HOLD signal is generated from the REQ signals by logic gate ~~236.Logic~~ 236. Logic gate 236 preferably comprises a logical OR gate. The HOLD signal is asserted if either or both of the request signals are asserted. The DMA arbiter 234 also receives both request signals, and in response it asserts a tentative grant signal TG1, TG2 for one of the DMA controllers. The tentative grant ~~signalsTG1,~~ signals TG1, TG2, for controllers 18, 28 are gated through logic gates 216, 226, ~~respectively.Gates~~ respectively. Gates 216, 226 preferably comprise logical AND gates. Logic gates 216, 226 respectively generate grant signals GNT1, GNT2 for controllers 18, 28 from the tentative grant signals TG1, TG2, and from a combined acknowledgement signal CHA. Logic gates 216, 226, assert their respective grant signals GNT1, GNT2 when both the tentative grant signal (TG1, TG2) and the combined acknowledgement signal CHA are asserted. The combined acknowledgement signal CHA is generated by logic gate 238, which asserts the combined acknowledge signal CHA only when hold acknowledgement signals HA1, HA2 from both processor cores are asserted. Logic gate 238 preferably comprises a logical AND gate.--